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EXAMINER	
WOODS, ERIC V	

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2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,636	YOSHIDA, YOSHIJI	
	Examiner	Art Unit	
	Eric Woods	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) [ ] Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, see Remarks pages 1-10 and various amendments, filed 27 February 2006, with respect to various objections and rejections have been fully considered and are persuasive.

The objections to the title, abstract, drawings, and specification all stand withdrawn in view of applicant's amendments to correct the deficiencies therein.

The changes as above are accepted.

All rejections against claims 1-12 stand withdrawn because those claims have been canceled.

New claims 13-24 are submitted.

All of applicant's Arguments are otherwise directed to patentability of the new claims over the applied references and thusly moot; they will be considered if those references are applied below, with the requisite added features covered.

Drawings

The drawings were received on 27 February 2006. These drawings are accepted.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 11/30/2005 and 5/11/2005 was filed after the mailing date of the Non-Final Rejection on 20 September 2005. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the examiner is considering the information disclosure statement.

Claim Objections

Claim 17 is objected to because of the following informalities: the term 'his' is used in the third clause, where this is clearly correct and is a typo.

Claim 17 is objected to because the word 'patter' is used in the second to last clause, where it is clearly misspelled and meant to be 'pattern'.

Appropriate correction is required.

Double Patenting

Applicant is advised that should claims 15 and 22 be found allowable, claims 16 and 23 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Applicant is advised that should claim 14 be found allowable, claim 19 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

The only difference between claim 14 and 19 is that the limitation of a first reading device (second item in claim 14) was removed. It is pointed out that such a device must inherently be present in any case, since the decoder must

obtain compressed image data from some source, which would inherently be a kind of memory. Therefore, because of inherency, the claims are duplicates.

Applicant is advised that should claim 13 be found allowable, claim 18 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

The same logic above with respect to the difference between claims 13 and 18 applies herein.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 13-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Specifically, as noted in the attached Office Actions from JPO, the claims include the feature that the first storage device is incapable of simultaneously performing the write operation and the read operation where a write operation is

given priority over a read operation. While the specification does discuss having first and second storages that are incapable of simultaneously performing read and write operations, it does not cover the priority claim. Indeed, the specification clearly **teaches away** from this implementation for the first storage ('sprite buffer' in the instant specification)(that is, read operation given precedence over write operation **as described in the specification**)

The actual specification states, in the Summary of the Invention section – page 2, last paragraph:

"In order to draw an image in association with the frame buffer, it is necessary to read sprite pattern data from the sprite buffer, wherein an **expansion access is given a first priority** in order not to unexpectedly break a decoding process in progress in the decoder ... "

Claims 13-24 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The priority of the write operation over the read operation, which is critical or essential to the practice of the invention and is the inventive improvement (see for example Brief Summary of Invention section of the specification), but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). Specifically, the priority of the read operation is extolled in the instant specification as superior and the inverse operation is disparaged. Therefore, this feature is critical and will not work for its intended purpose **if the write operation is used first**. The specification clearly utilizes the reverse method.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito (JP 2002-341859, supplied by applicant on IDS-see attached translation of specification-paragraphs are numbered and referenced accordingly below) in view of Xie (US PGPub 2005/0024369 A1), Snyder et al (US 6,326,964 B1), and Witzig (NPL used in last OA).

As to claim 13,

An image processing device comprising:

-A first reading device for reading compressed image data, each of which are compressed into blocks in advance, from a memory; (Ito [0022] teaches that using compressed data for sprite creates more efficient bus transfers; sprites are stored in a pattern ROM 25 (see Figure 2) [0013-0015], which constitutes the

'memory' recited. Such compression could be in block form, as is well known in the art, because block format is easier to access and requires less space in the memory address table. All such compression is done in advance, since a ROM cannot be written to. Next, see Figure 1, where readout circuitry 28 and 29 read data and generate address from the pattern ROM, particularly 28 [0014-0015]. Note that such data can be run length compressed [0023], which usually occurs in block format.)(Snyder et al teaches that sprites are held in a compressed cache (element 458, Figure 12A), where the sprite data is in block format, which would constitute the 'a memory' recited in the above claim; see Figure 12A-12B, 28:44-67, which explains block process and 27:40-28:43, which explains generic system operation. Snyder inherently has readout circuitry for the cache, as in Figure 12A such a path is shown from the compressed cache through the decoder to the main sprite cache, where images are formed in tiles (see tiler 200 in Fig 4A, which feeds into Gsprite engine 204, which is shown as block 436 in Figure 12A).)

-A decoder for decoding the compressed image data in units of blocks so as to decompress image data; (Ito must have a decoder for decompressing the data from the sprite pattern [0020-0023]; see element 30 in Figure 1, which can perform this task [0015-0016]. The term 'defrosting' is a machine-translated term meaning 'decompressing' in that context.)(Snyder has a decoder for block data that decompresses such data in Figure 12A, see decompression engine 450, as described in 28:15-35)

-A first storage device that is given a priority in a write operation rather than a read operation and is incapable of simultaneously performing the write operation and the read operation; (Ito teaches a sprite buffer 33 in Figure 1 [0016], which constitutes a 'first storage device,' which is implemented as a dual port RAM [0019], which is normally implemented with a single port RAM emulating a dual port RAM. Further, the Ito reference clearly teaches that it is optimal to have a sprite buffer because it increases the data throughput [0021-0023], and that data reads should get priority [0017-0018], where this is suggested because of the fact that data must be read from the sprite buffer to the frame buffer to be written to the display, where it would be obvious that such data that any reads from data in the sprite buffer are going to be faster than write commands from the pattern ROM, which constitute write operations **to** the sprite buffer, because any request for data from the pattern ROM must be decoded and then passed to the sprite buffer, meaning that it will always maximize data transfer to pull data from the sprite buffer first because it takes less time for that data to be written to the frame buffer [0022]. Finally, as noted above, since the frame buffer needs to read data in order to display it to the user, *prima facie* that means that the source of data being read (e.g. the sprite buffer) needs to write data, and that write operations should occur before read operations. The above logic applies if it were implemented as a **single-port** RAM, which would therefore justify a preference for write operations)(Xie teaches that a single port RAM [0902-0916] can be used to emulate a dual port RAM, since the single port RAM is much cheaper, takes up 30-40% less area, and the like. A single port RAM inherently only performs

one type of operation at a time, where such can be applied to graphics buffers and the like [0916])

-A writing device for writing the decompressed image data into the first storage device; (Ito Figure 1 shows element 30, the real-time image decompressor, that writes such data to the sprite buffer, since it decompresses the data, as explained above in [0022], and that is the data path)

-A second reading device for reading the image data from the first storage device; (Ito Figure 1 has circuit 37, which reads data from the sprite memory 33 [0017]; also element 33 passes data to the frame buffer, so there must inherently be a reading device present. Finally, elements 35-36 read display position and generate the relevant addresses)

-A second storage device that is given a priority in a read operation rather than a write operation and is incapable of simultaneously performing the read operation and the write operation; (Ito Figure 1 contains frame buffer 39 in two-port mode. Clearly such a device should have a preference for read mode, as explained above with respect to the sprite buffer. As the sprite buffer should preferentially write, the frame buffer should preferentially read data if it were implemented as a single-port RAM)(Xie clearly provides that a single port RAM that can be used to emulate a two-port RAM for use as a frame buffer [0916], and also for the reasons stated above (savings of area and cost [0902] and improvements in bandwidth [0015])

-A control device for performing prescribed processing on the image data from the first storage device so as to produce processed image data, which are then

written into the second storage device; and (Ito Figure 1 contains element 37, which is a rendering processing circuit that takes sprite data and performs rendering processes such as rotating a sprite from the sprite cache by ninety degrees (equivalent to 'prescribed processing' in above claim clause. Ito then takes such data and writes it to the frame buffer [0017] once it has been processed.)

-A display device for reading the processed image data from the second storage device, thus displaying an image based on the processed image data, wherein (Ito teaches a display device 26, where the frame buffer data is written to such a display when read from the monitor [0018], which can be a LCD monitor (Figure 2))

-The first storage device serves as a first-in-first-out memory and is controlled by way of the writing device and the second reading device. (Xie teaches that the single-port RAM is good for implementing a FIFO [0916], and contains display FIFOs ([0183, 0890-0891, 0917]), where such buffers have advantages for improving bandwidth)(The system of Ito therefore is controlled by the rendering device 37, which implements calls to the pattern ROM to obtain sprites not found in the sprite buffer [0016-0018, etc].)(Snyder at least suggests using FIFOs as caches, particularly when a FIFO is used as a pixel cache in 21:5-55 where that is for a texture cache, where a texture can be viewed as a type of sprite)(Witzig pages 1-2, where it is stated that a FIFO is a ring buffer with a read and write pointer. FIFOs reside in shared memory and any process after an initial attachment to the FIFO system can read and write into any FIFO (e.g. sprite

buffer, since sprite buffers are in shared memory (RAM)). Further, semaphore operations can implemented that guarantee that only one process accesses one FIFO at a time. FIFOs implemented in this manner have several advantages for event distribution among an arbitrary number of processes: once an event is in the FIFO, only an object or structure is passed between processes. Once a process takes such a structure out of a FIFO, it is guaranteed that no other process can access this object by mistake. A CPU intensive stage can be done by several processes in parallel, and many other options as stated therein))

Ito teaches all of the limitations of the reference above, except that the compressed data is stored in block format (although RLE data is stored in line format, which would at least suggest the use of blocks, where a line could be considered a block), that the buffers (first and second storage) are not capable of simultaneous read and write access, and that buffers should preferentially be FIFOs. The Snyder reference provides that storing such data in block format is preferential because of spatial locality; namely, textures are stored as 8x8 blocks (as per 21:9-22:15), wherein this is done because block transfers from cache to DRAM and back maximize DRAM bandwidth utilization and the lowest miss rates for the cache occur when the block size matches the cache line size. Again, textures are graphics data, and clearly gsprite blocks are texture blocks (28:52-67, as an example). All of the above are well known in the art.

Next, Snyder provides examples of how FIFOs can reduce latency in certain circumstances, Xie states that FIFOs can be used as buffers in certain

circumstances, and Witzig clearly shows why using FIFOs as buffers is beneficial.

Finally, Xie provides evidence that single port RAM implementations that emulate dual-port RAM are advantageous, and single port RAM inherently can only perform one operation – read or write – at a time, where motivation for doing so has already been discussed above.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Ito, Snyder, Xie, and Witzig with Ito in the manner above, with the above described modifications, for the reasons provided above.

Also, as evidence that such is well known in the art (in terms of making the read and write interactions between a first memory and a second memory synchronous and the like as being more efficient), note the following from the last office action. These serve as evidence claims. The following is provided as proof that maximizing read and write cycle synchronization between two memories is well known in the art, and the reasons for doing so are further well known. The Yamashita and Takahashi references would serve as the required proof of the facts and motivation. (Yamashita (9:5-3) teaches that timing commands between a first and second memory are synchronized such that read and write operations occur opposite to each other as stated in the above claim, and teaches that such synchronization is clearly beneficial because it allows read and write operations to occur in parallel. The overall system of Yamashita is clearly directed to a method of synchronizing read and write signals, and prior art

performs such steps as well, where such synchronization is performed because it is more efficient and more economical)(Takahashi teaches that synchronizing read and write signals results in a more economical memory.)

As to claim 14, this is very similar to claim 13, the rejection to which is incorporated by reference in its entirety.

The different limitations are described below, and addressed:

-A sprite attribute table for storing sprite attributes (Ito Figure 1, element 23 is the sprite attribute table [0014]; motivation for having such is found in [0010-0012] as an example.)

-A first reading device for reading compressed image data ... by referring to said sprite attribute table (Ito teaches that the data is read from the sprite ROM / memory 25 in Figure 2, and the sprite attribute table 23 in Figure 1 is generated by CPU 22 in Figure 2, where the sprite attribute table is used to read such data from the sprite attribute table by utilizing it to obtain memory addresses for the actual sprite ROM to load such into the sprite cache utilizing address circuitry 28-29 to obtain RAM data from 25)

As to claims 15 and 16, Ito clearly teaches that the rendering circuit 37 performs rotation upon obtained image data [0017].

As to claim 17, this is merely a method implementing the apparatus of claim 14, where the steps correspond to each element therein. The rejection to

claim 14 is therefore incorporated by reference in its entirety, and is equally applicable upon this claim.

As to claim 18, this is merely claim 13 with a slight variation, which is addressed below. The rejection to claim 13 is incorporated by reference in its entirety.

The reading device is the second reading device of the rejection claim 13.

The only difference between claim 13 and 18 is that the limitation of a first reading device (first item in claim 13) was removed. It is pointed out that such a device must inherently be present in any case, since the decoder must obtain compressed image data from some source, which would inherently be a kind of memory. Therefore, because of inherency, the claims are duplicates.

Next, the decoder generates sprite data – it is noted that in Ito, the compressed data **is** sprite data, so prima facie the recited decompressed image

Additionally and alternatively, the omission of an element and its function is an obvious expedient if the remaining elements perform the same functions as before – see *In re Karlson* (CCPA) 136 USPQ 184 (1963).

As to claim 19, this is merely claim 14 with some slight variations, which are addressed below. The rejection to claim 14 is incorporated by reference in its entirety.

The reading device is the second reading device of the rejection claim 14.

The first difference is the removal of the element / limitation of a first reading device. It is pointed out that such a device must inherently be present in

any case, since the decoder must obtain compressed image data from some source, which would inherently be some kind of memory.

Next, the decoder generates sprite data – it is noted that in Ito, the compressed data **is** sprite data, so prima facie the recited decompressed image data and sprite data are the same thing.

As to claims 20 and 21,

The references do not expressly teach all limitations, but either inherently contain them or fairly suggest or them as below.

As to the limitation that the display controller starts to read the display from the second storage at a timing that allows the display data of one line to be read out, Snyder teaches that the display device utilized is a conventional CRT display [the same thing applies to LCD displays, which utilize similar readout techniques](an LCD could obviously be replaced by a CRT; they are both standard types of displays that are well known in the art), which scans one line at a time, top to bottom. Ito discusses the use of line buffers in [0023], where display devices utilize those for writing such data. Therefore, Snyder inherently teaches that the display controller would read data one line at a time from the frame buffer. Also, inherent in the way CRTs operate is that there is are Vsync and Hsync (vertical and horizontal synchronization) signals that, in order to be displayed correctly, the display device must match the vertical and horizontal write rates set by those sync signals, or else convert those signals to another video format with different sync rates that match that of the monitor. The VGA standards family uses a common sync rate, and most monitors therefore support

that mode, where lines are read from the frame buffer and written to the display at a rate specified by the Vsync signal. This may be modified (as in Yamashita) by using line buffers or the like, as is trivially well known in the art, and it would be obvious to do so (if necessary) as set forth in Yamashita, which is already part of the rejection.

As to the limitation that the reading "is counted backwardly from a start timing of a horizontal display period of the device", the Hsync (or horizontal synch) signal for a display device sets the rate of reading from one line of the display and thusly sets the rate of counting. The start timing provided by the elapse of one time period between Vsync signals causes a new start signal for reading a new line of the frame buffer, and that signal constitutes 'a horizontal display period of the device'. As to the limitation of reading backwards, this is a matter of design choice (see *In re Gazda,* 219 F.2d 449, 104 USPQ 400 (CCPA 1955)) where the direction of reading is a moot point (reversal of parts as obvious expedient). Specifically, applicant has not disclosed an advantage for this limitation or shown any criticality. As such, the direction of reading (right to left or left to right) provides no technical advantages, and there have been many displays and hardware that read in both directions. Further, depending on the nature of the memory and computer (e.g. whether or not the system was big-endian or little-endian), it might be read in reverse order anyway. It would have been obvious to read the buffer in the direction supported by the hardware (which can be either big-endian or little-endian, which therefore means that the read direction is hardware variable in any case).

As to proof of both of the above, see Giloi (Wolfgang K. Giloi. "Interactive Computer Graphics: Data Structures, Algorithms, Languages". Pages 246-248). Further see Broemmelsiek (US 5,574,836)(7:1-12, 18:62-19:10) and Hannah (US 5,345,252)(2:3-15,7:65-8:67) for proof that both of the above are old and well known in the art.

As to the limitation that "in a time period in which the sprite pattern data is not written to the first storage, the display controller starts to read..." the display **must** operate in the manner specified above. It is inherent to the operation of a CRT that the display controller will read data at a given timing, and in CRTs, the data is pulled from the frame buffer, regardless of what the first storage is doing. (Also, there are enablement problems with this wording, see above – it does not make sense that the display would read only when the sprite patterns are not written into the first storage). But in any case, it is an obvious expedient that whenever there is bus latency, that data should be transferred in order to maximize use of the bus and available resources. Obviously, transmitting the data in this 'down time' is old and well known in the art.

Therefore, the limitations of the above claim are met by the instant references and/or are rendered obvious, and/or shown to be implemented (or probably implemented) in holdings of inherency with respect to elements of the already-cited references.

As to claims 22 and 23, Ito clearly teaches that the rendering circuit 37 performs rotation upon obtained image data [0017].

As to claim 24, this is merely a method claim implementing the apparatus of claim 19. The rejection of that claim is herein incorporated by reference in its entirety.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 5/11/2006 prompted the new ground(s) of rejection presented in this Office Action.

Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Woods whose telephone number is 571-272-7775. The examiner can normally be reached on M-F 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eric Woods

June 30, 2006

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER